



US 20070063936A1

(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0063936 A1**
(43) **Pub. Date: Mar. 22, 2007**(54) **ORGANIC LIGHT-EMITTING DIODE
DISPLAY**(75) Inventors: **Kwang-Chul Jung**, Seongnam-si (KR);
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LTD.**, Suwon-si (KR)(21) Appl. No.: **11/557,244**(22) Filed: **Nov. 7, 2006****Related U.S. Application Data**(63) Continuation-in-part of application No. 11/204,042,
filed on Aug. 16, 2005, which is a continuation of
application No. 10/732,280, filed on Dec. 11, 2003,
now Pat. No. 6,946,791.(30) **Foreign Application Priority Data**

Nov. 15, 2005 (KR)..... 10-2005-0109063

Dec. 11, 2002 (KR)..... 10-2002-0078744

Publication Classification(51) **Int. Cl.**
G09G 3/30 (2006.01)(52) **U.S. Cl.** **345/76**(57) **ABSTRACT**

An organic light-emitting diode (OLED) display includes a substrate, an auxiliary electrode disposed on the substrate, a first signal line disposed on the substrate, a second signal line crossing the first signal line, a driving voltage line disposed on the substrate, a first thin film transistor connected to the first signal line and the second signal line, a second thin film transistor connected to the first thin film transistor and the driving voltage line, a first electrode connected to the second thin film transistor, a second electrode facing the first electrode, and a light-emitting member disposed between the first electrode and the second electrode. The auxiliary electrode is connected to one of the driving voltage line and the second electrode.

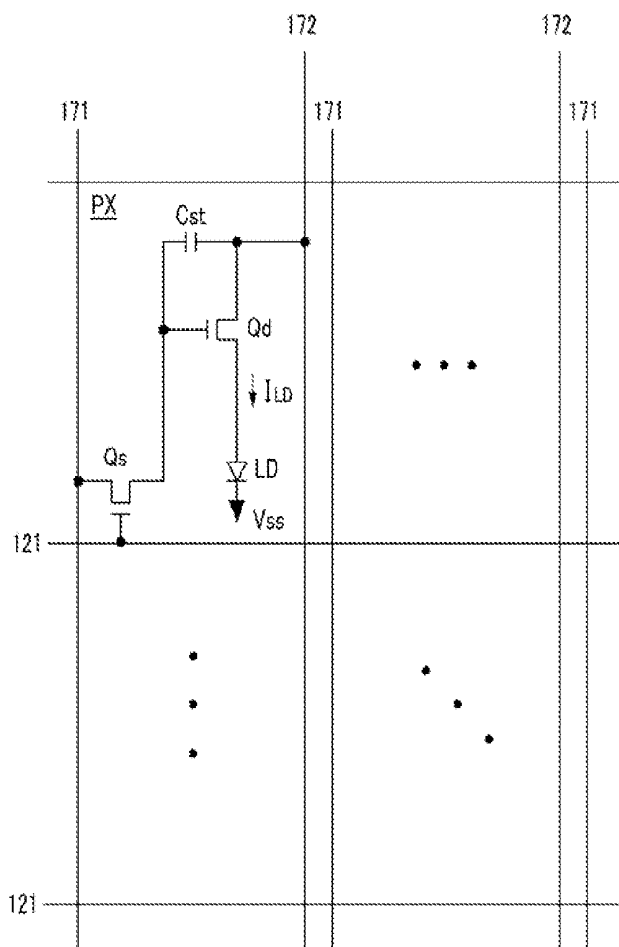


FIG. 1

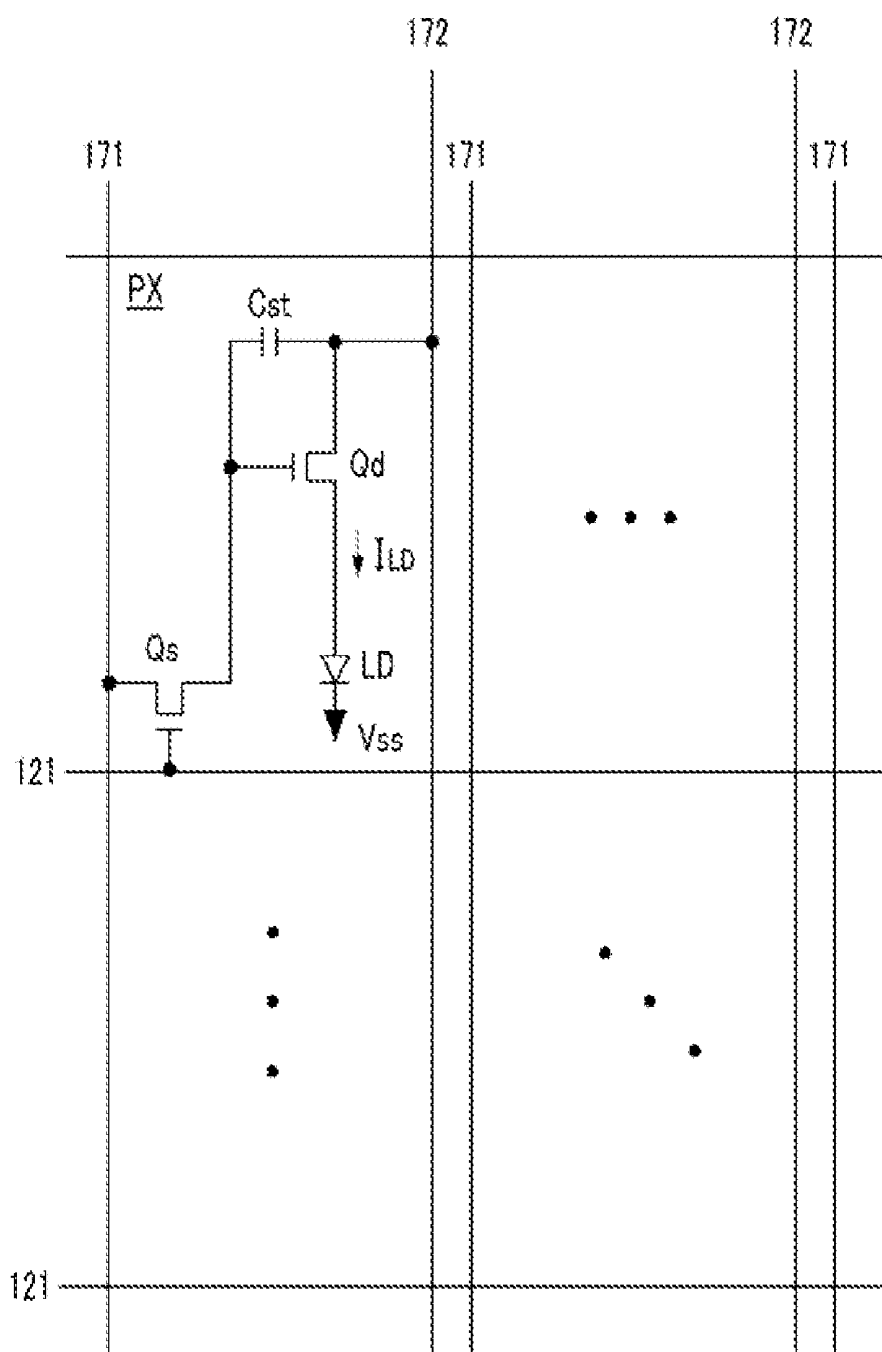


FIG.2

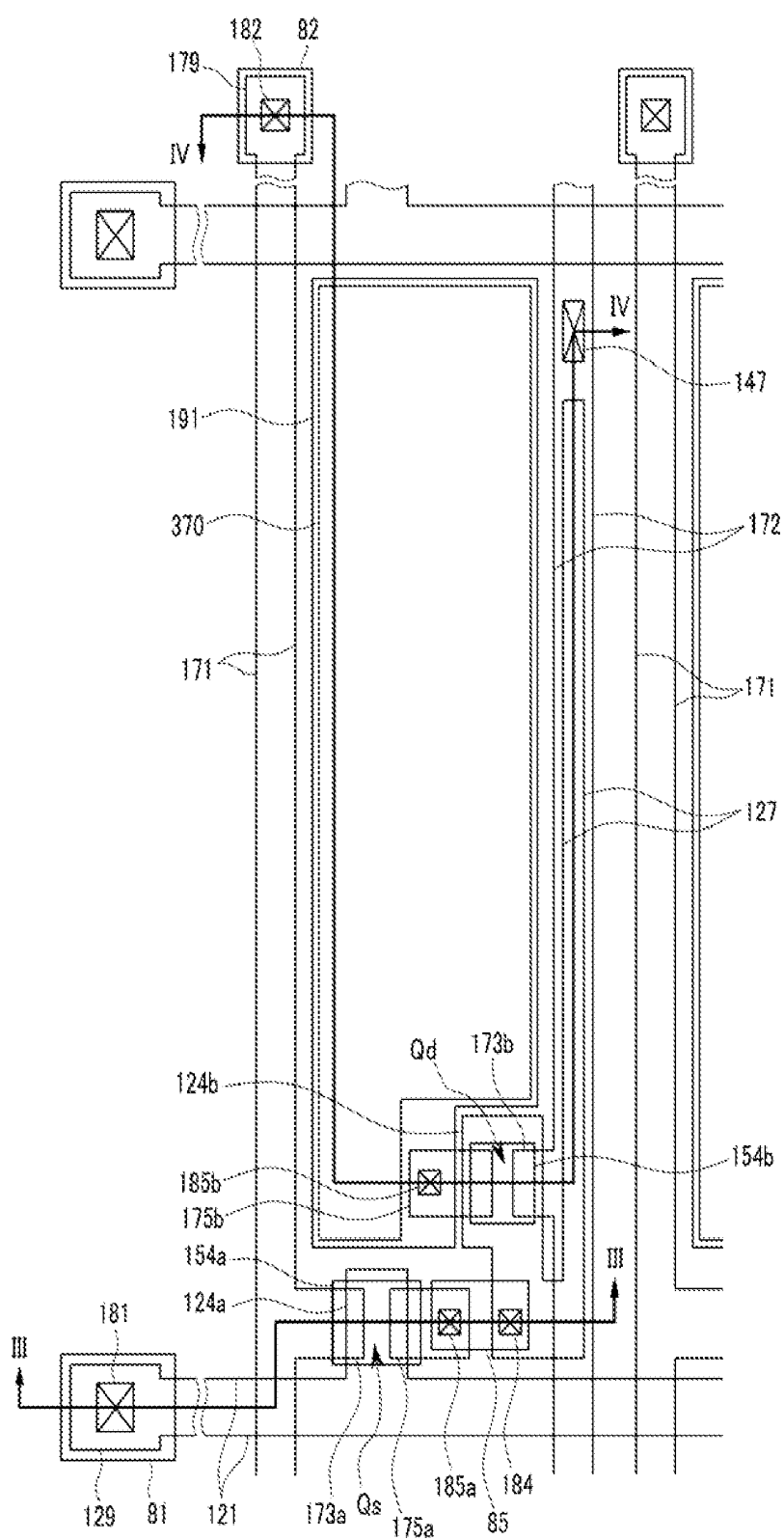


FIG.3

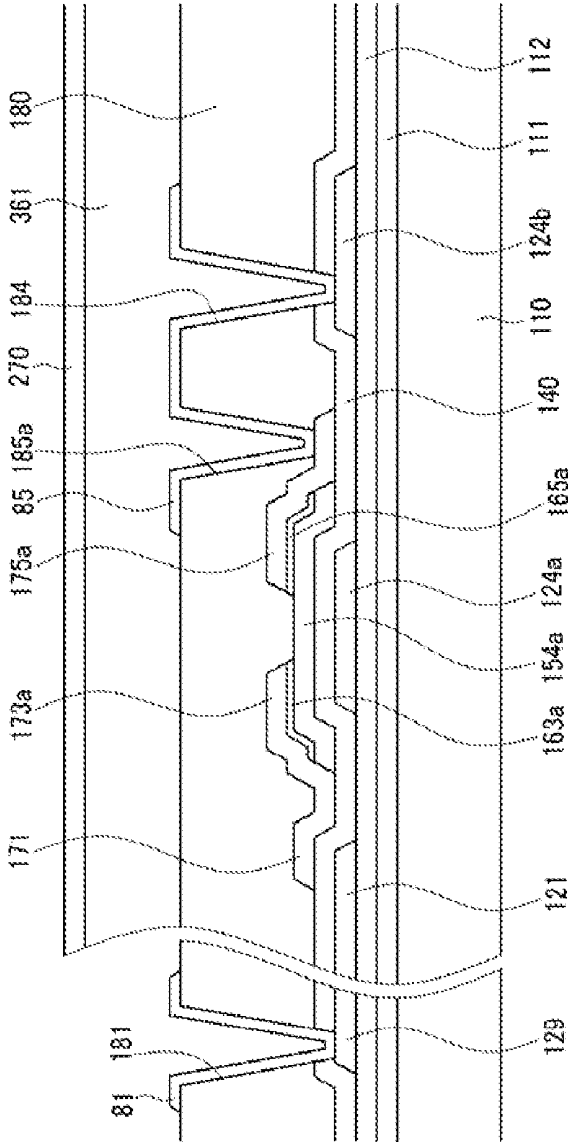


FIG.4

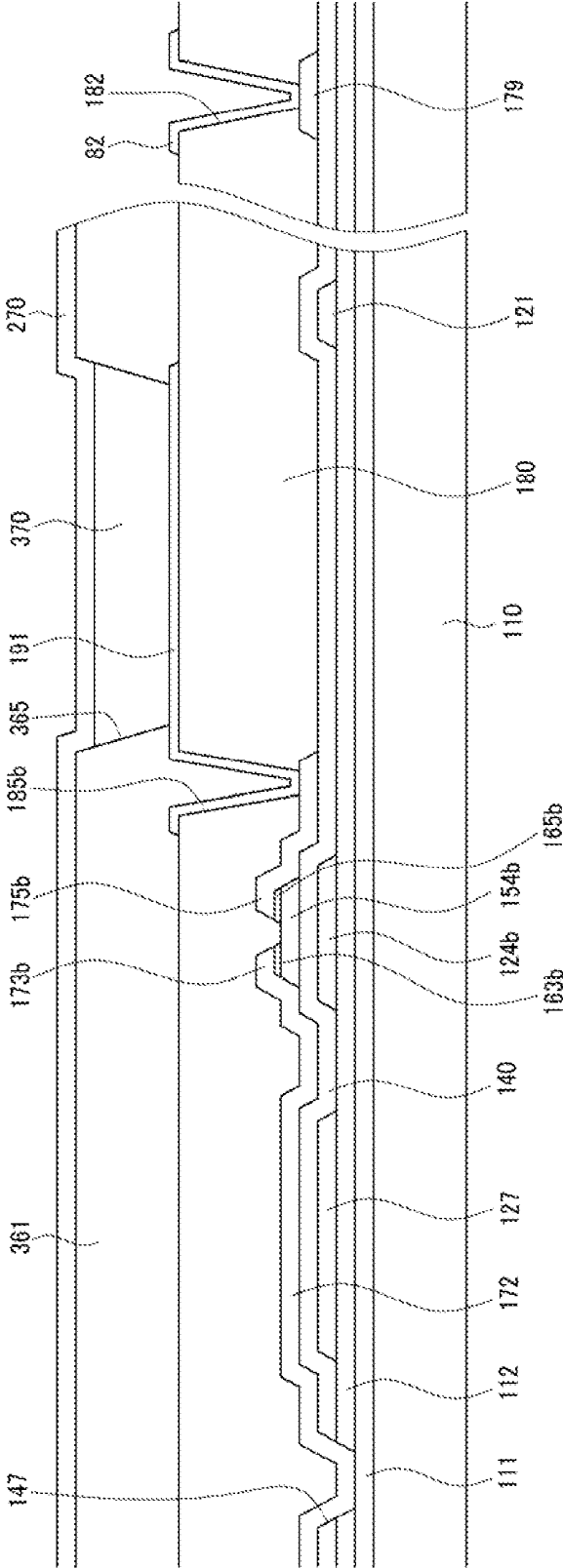


FIG.6

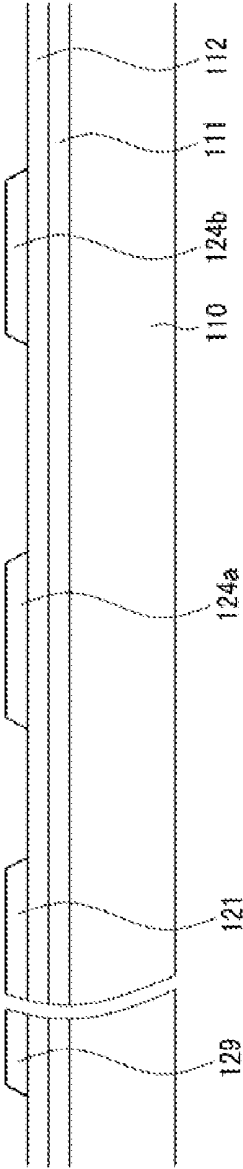


FIG. 7

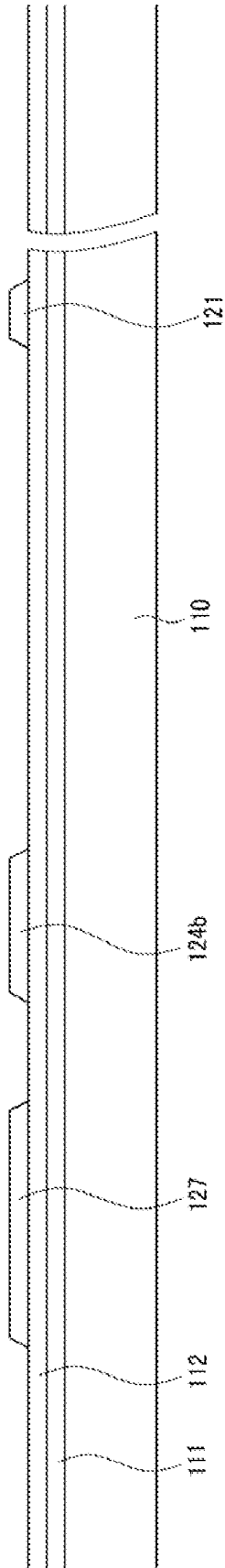


FIG.9

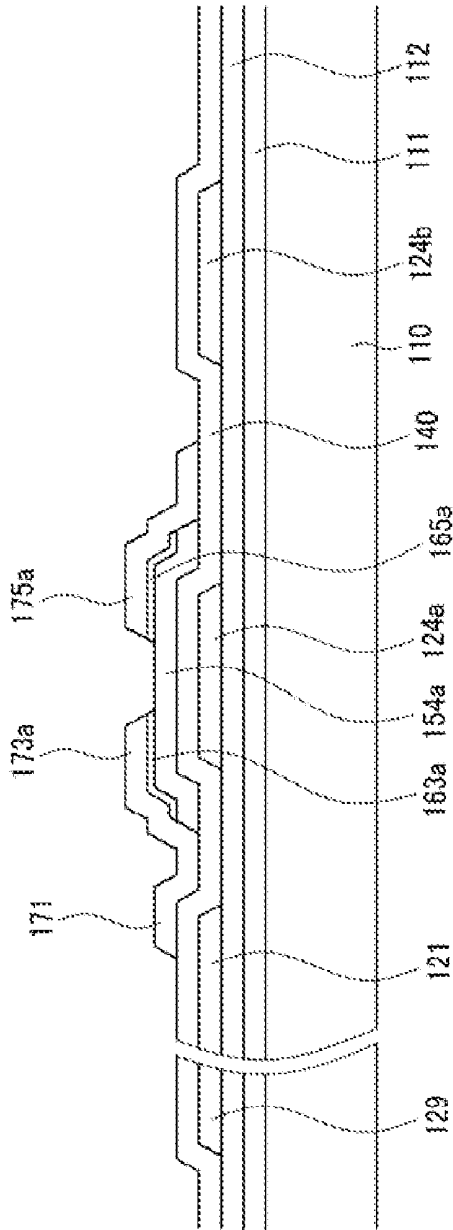


FIG.10

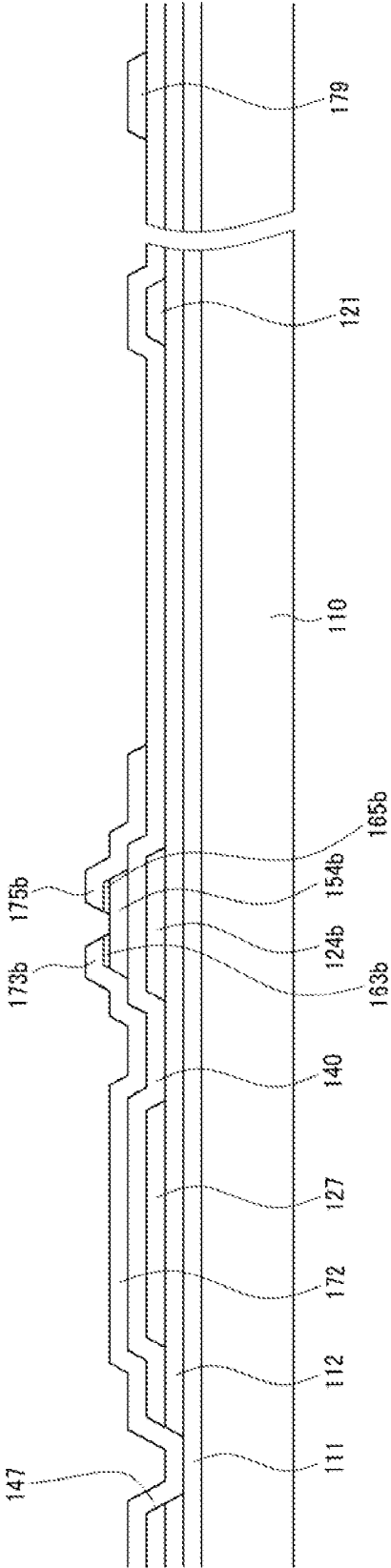


FIG.11

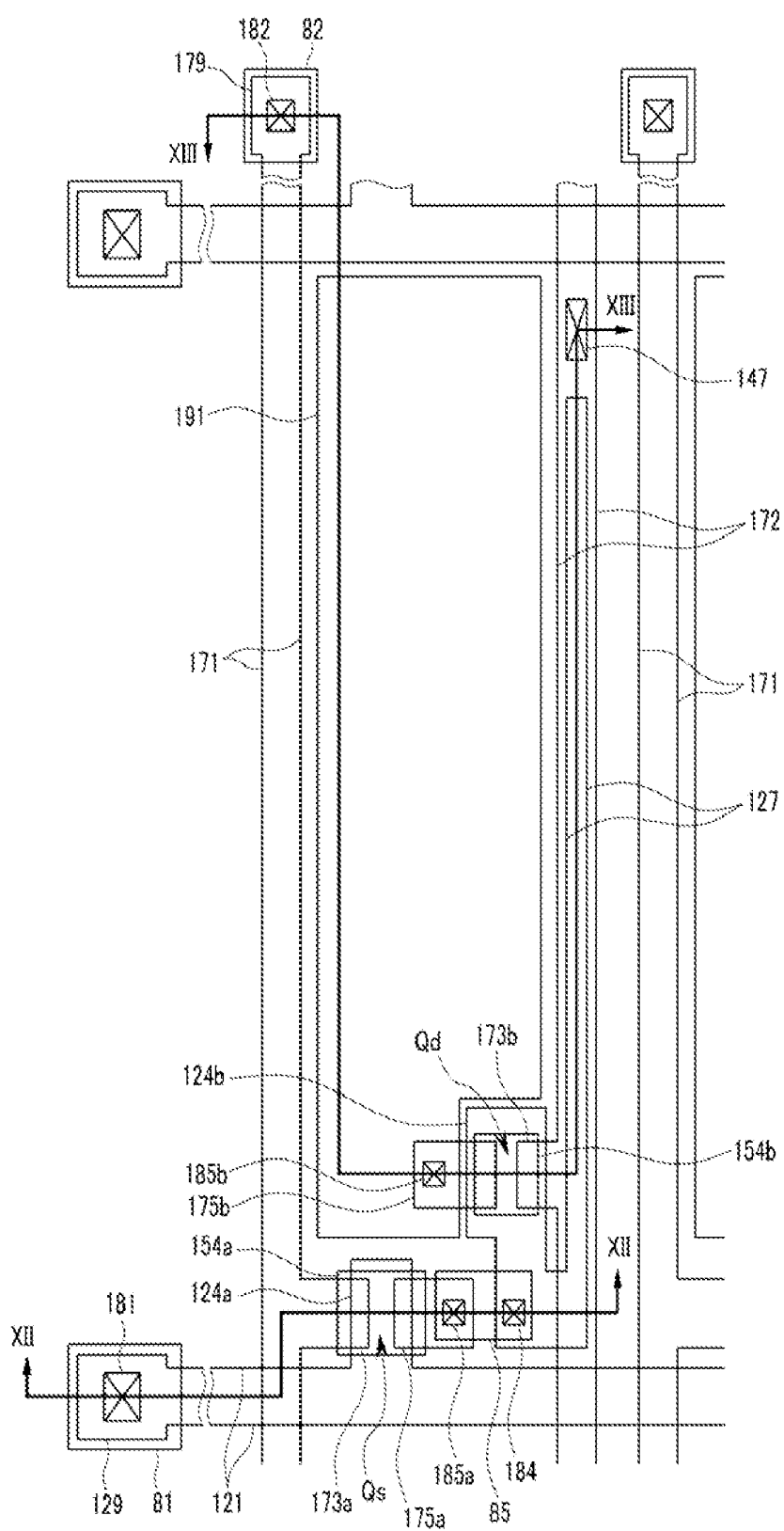


FIG.12

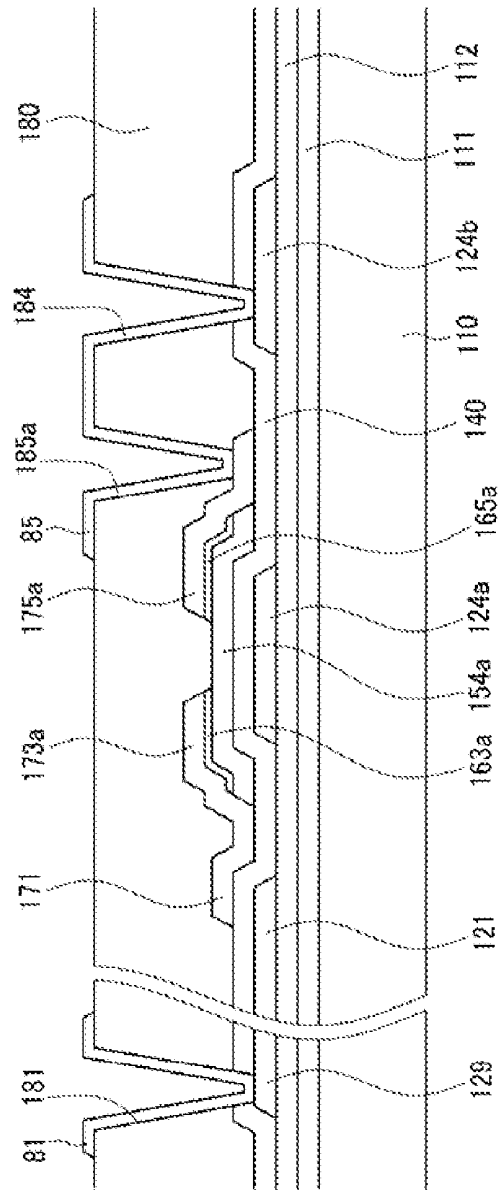


FIG.13

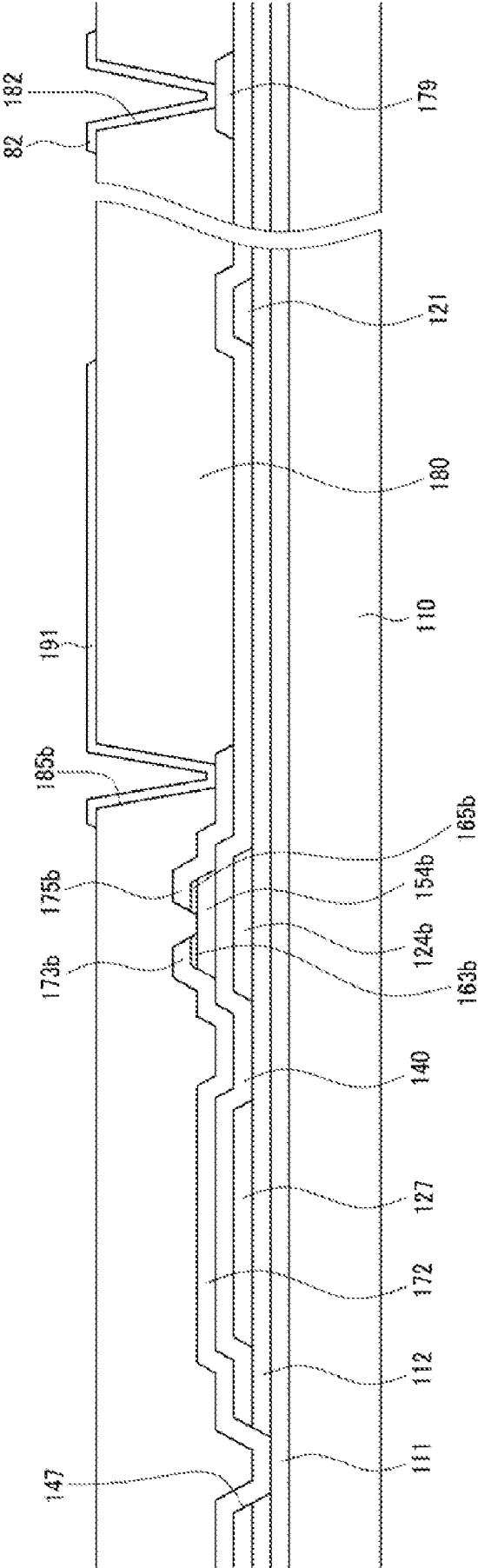


FIG.14

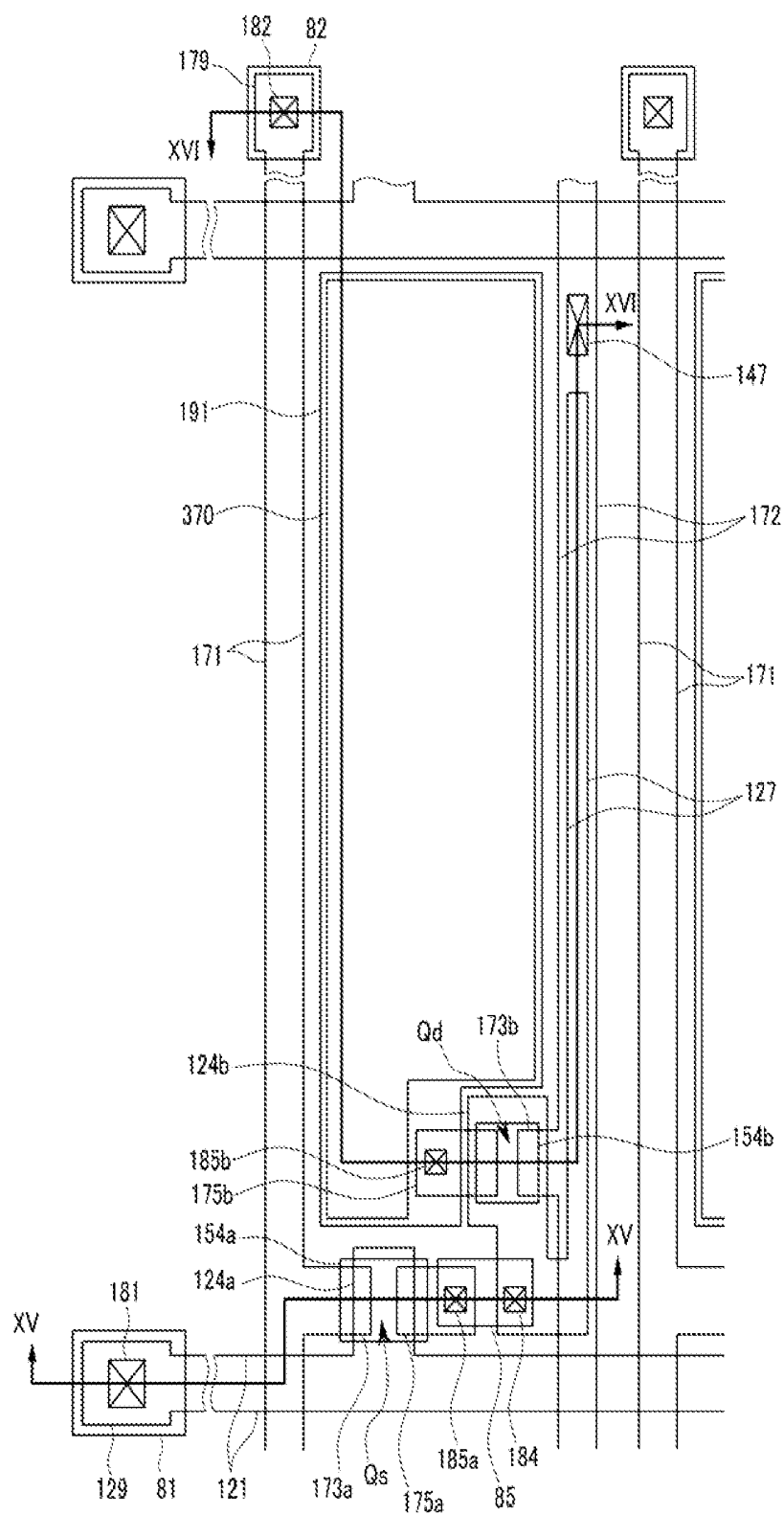


FIG.15

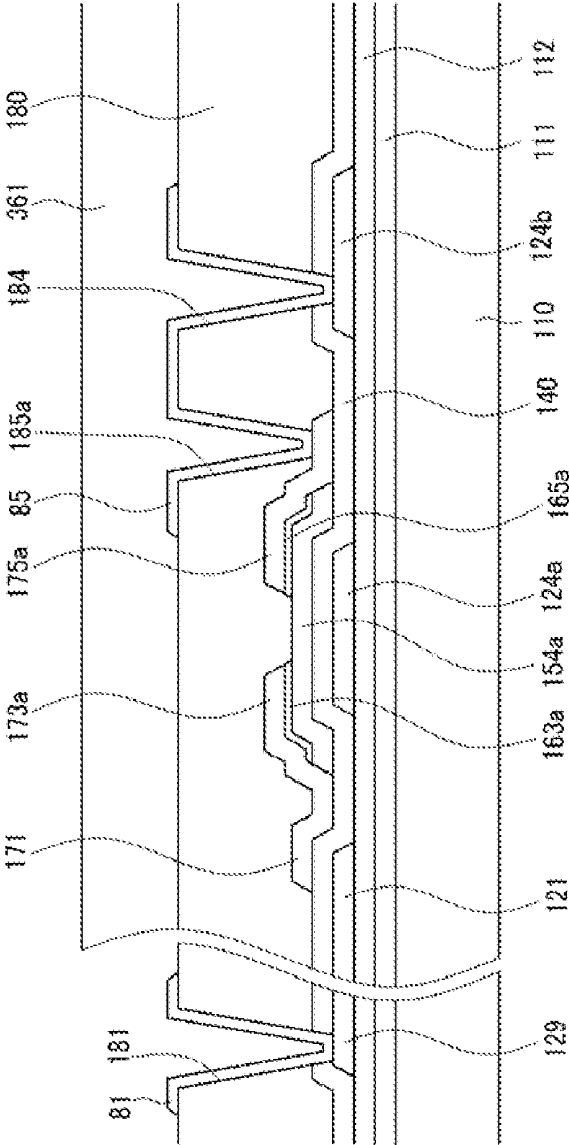


FIG.16

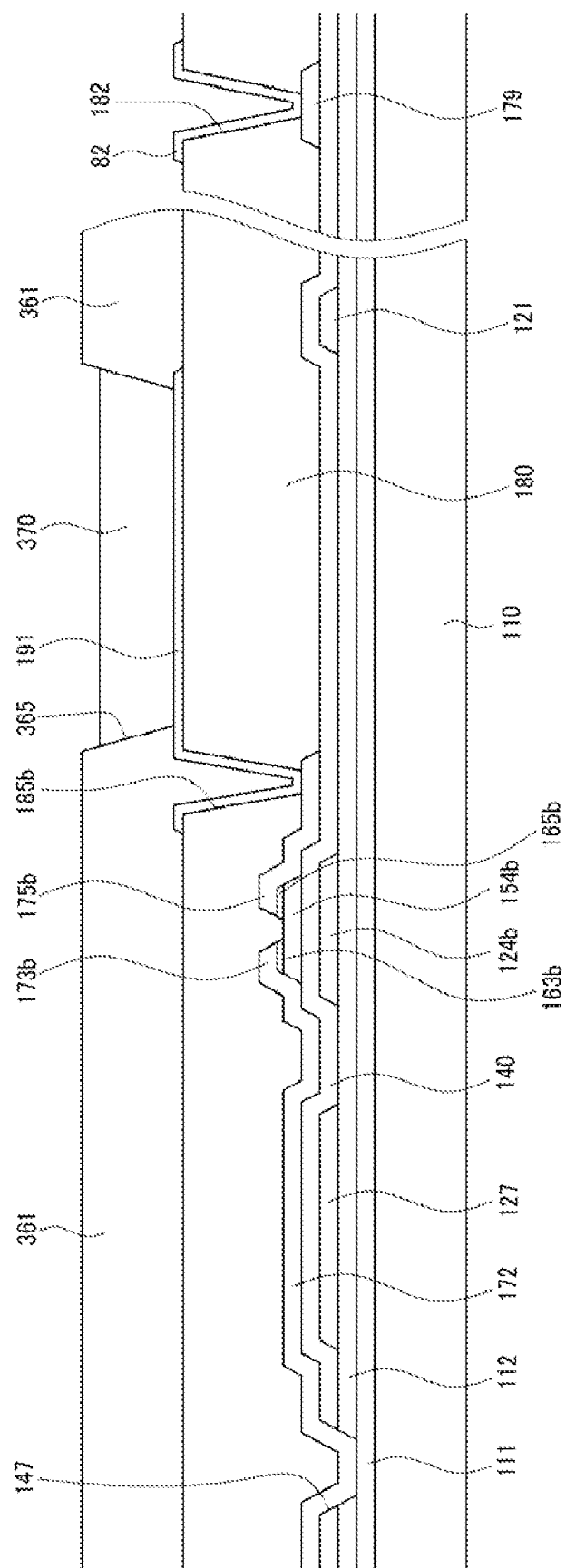


FIG. 17

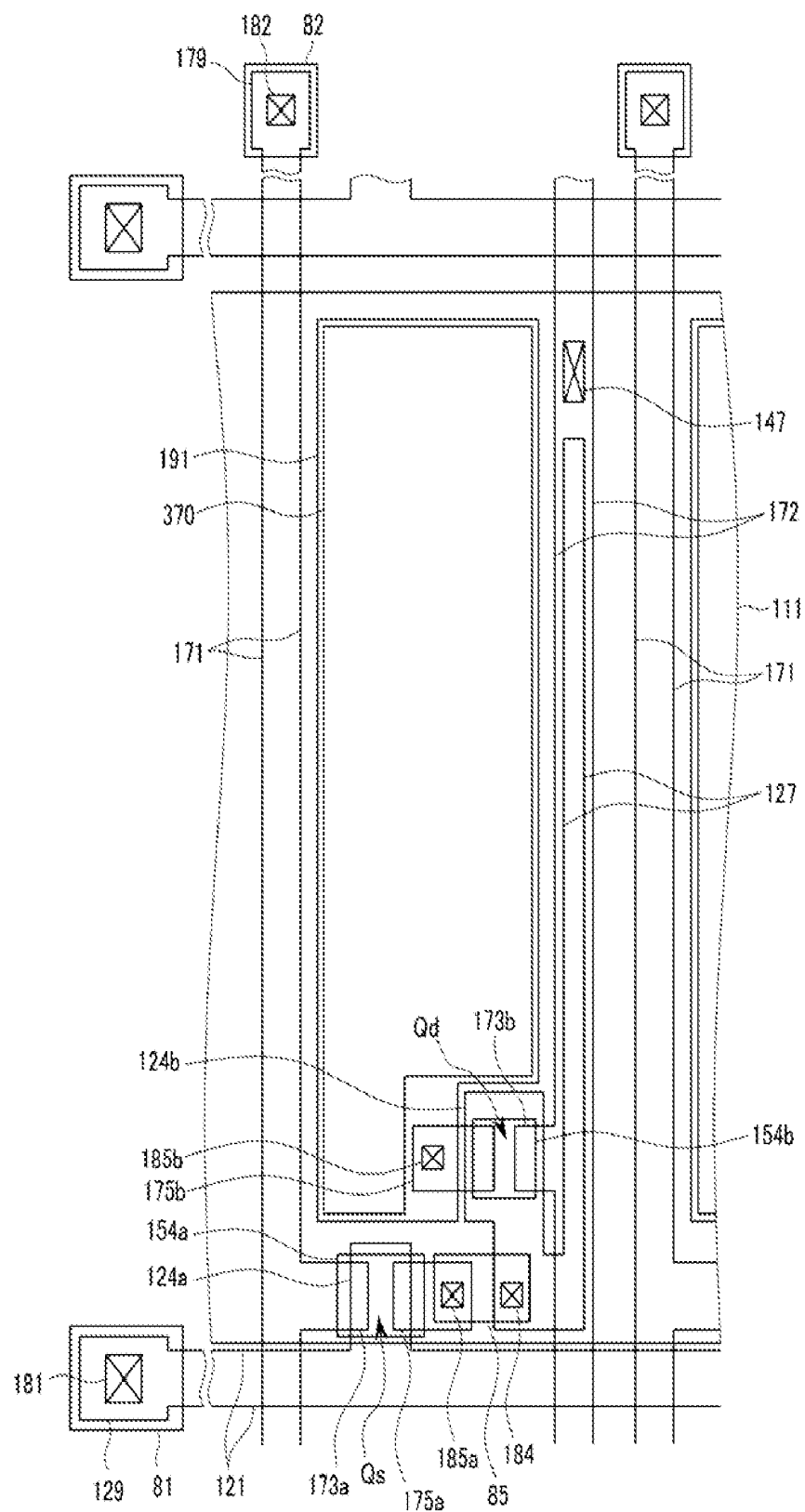


FIG.18

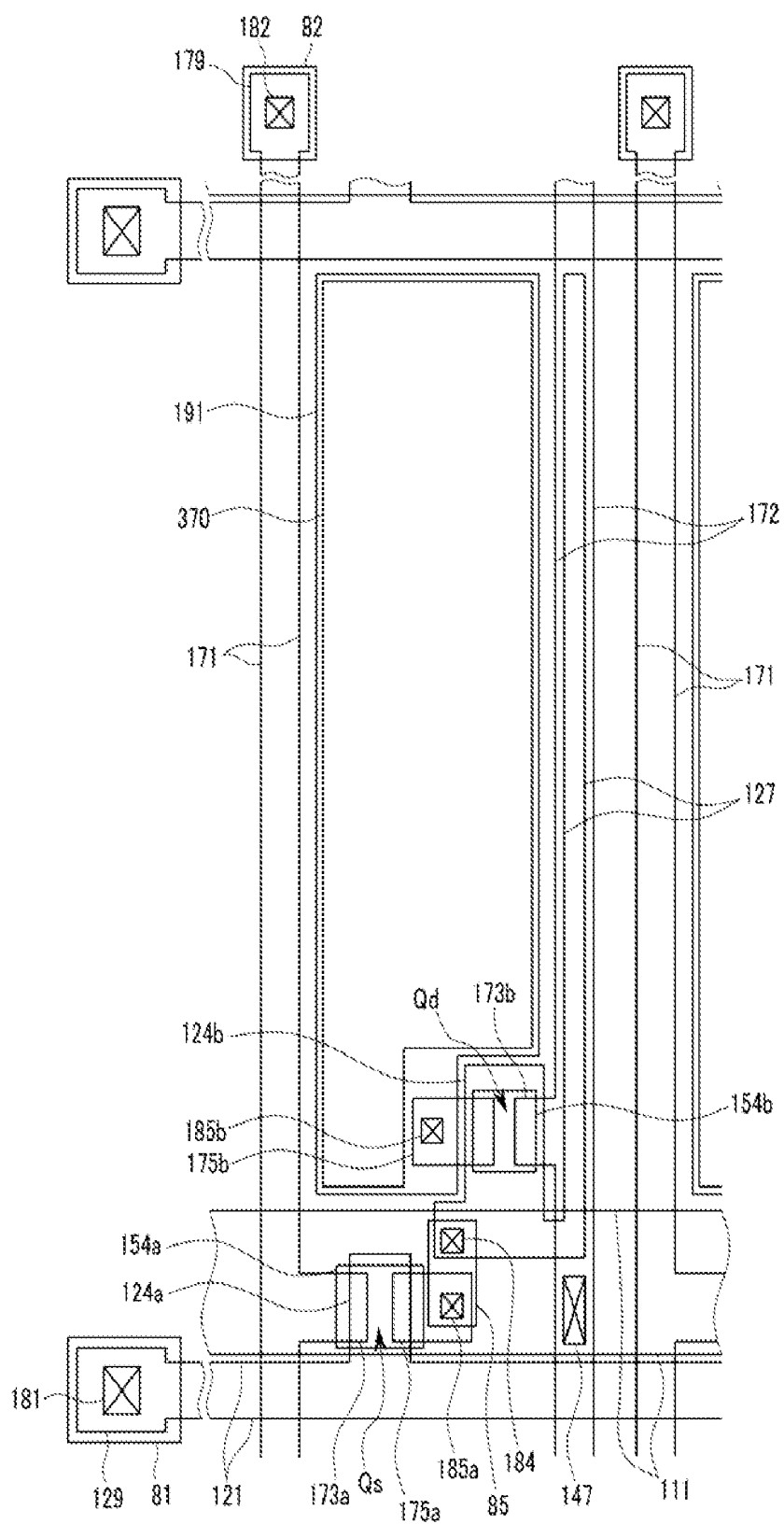


FIG.19

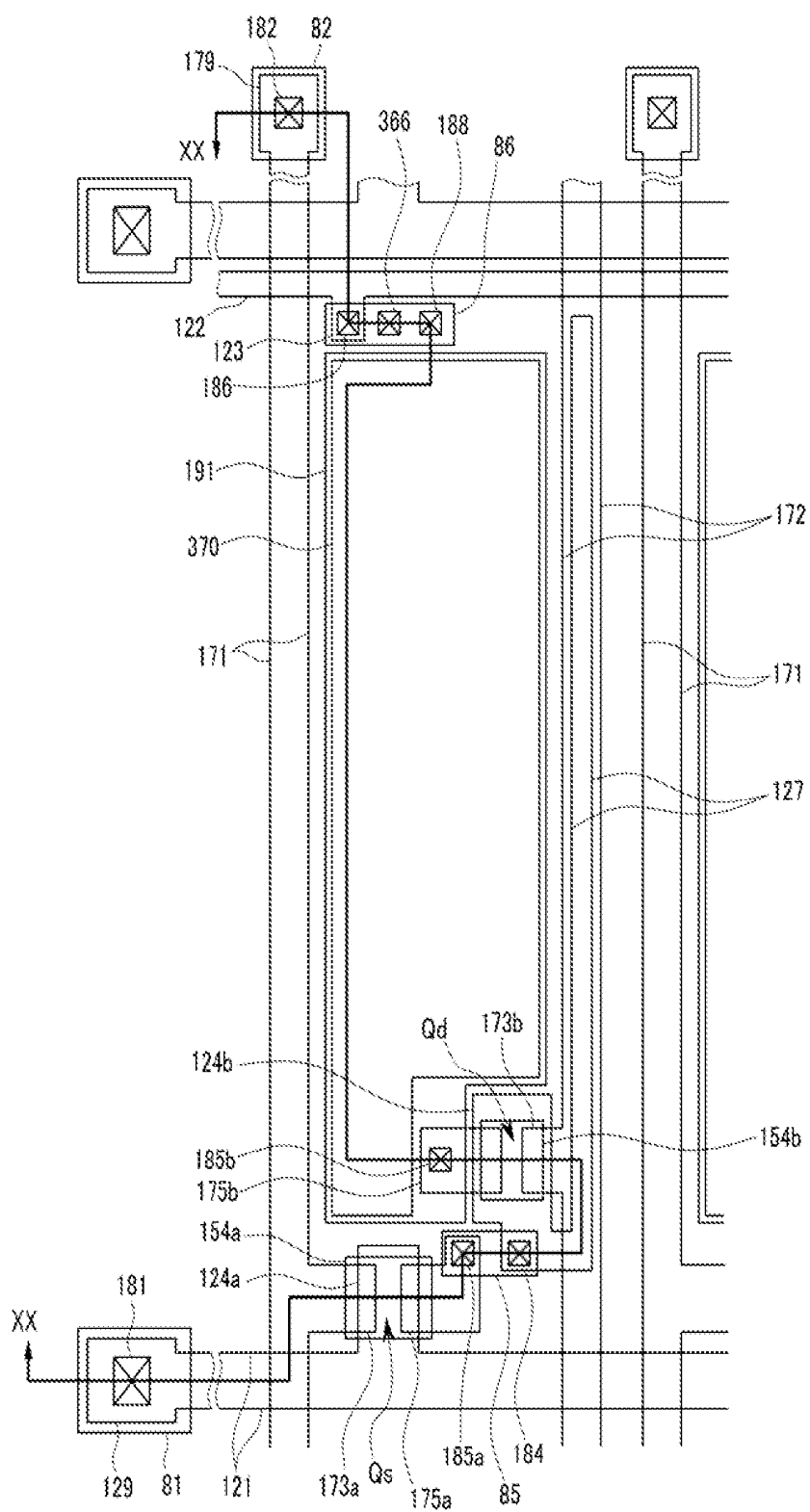


FIG.20

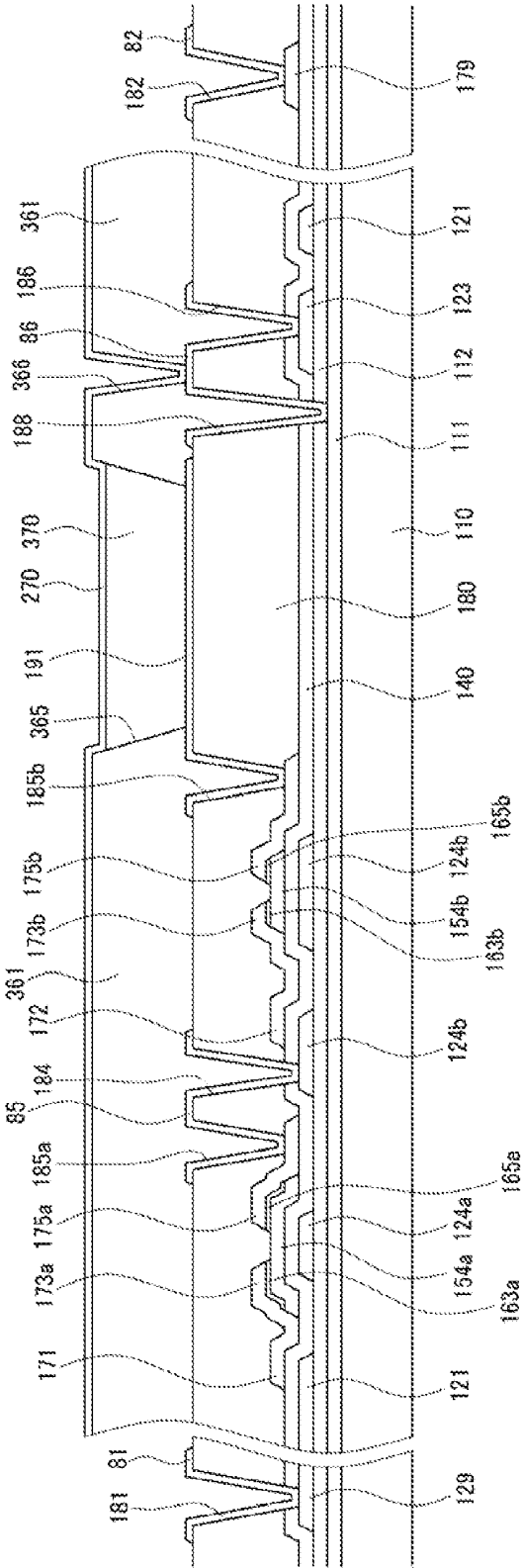


FIG.21

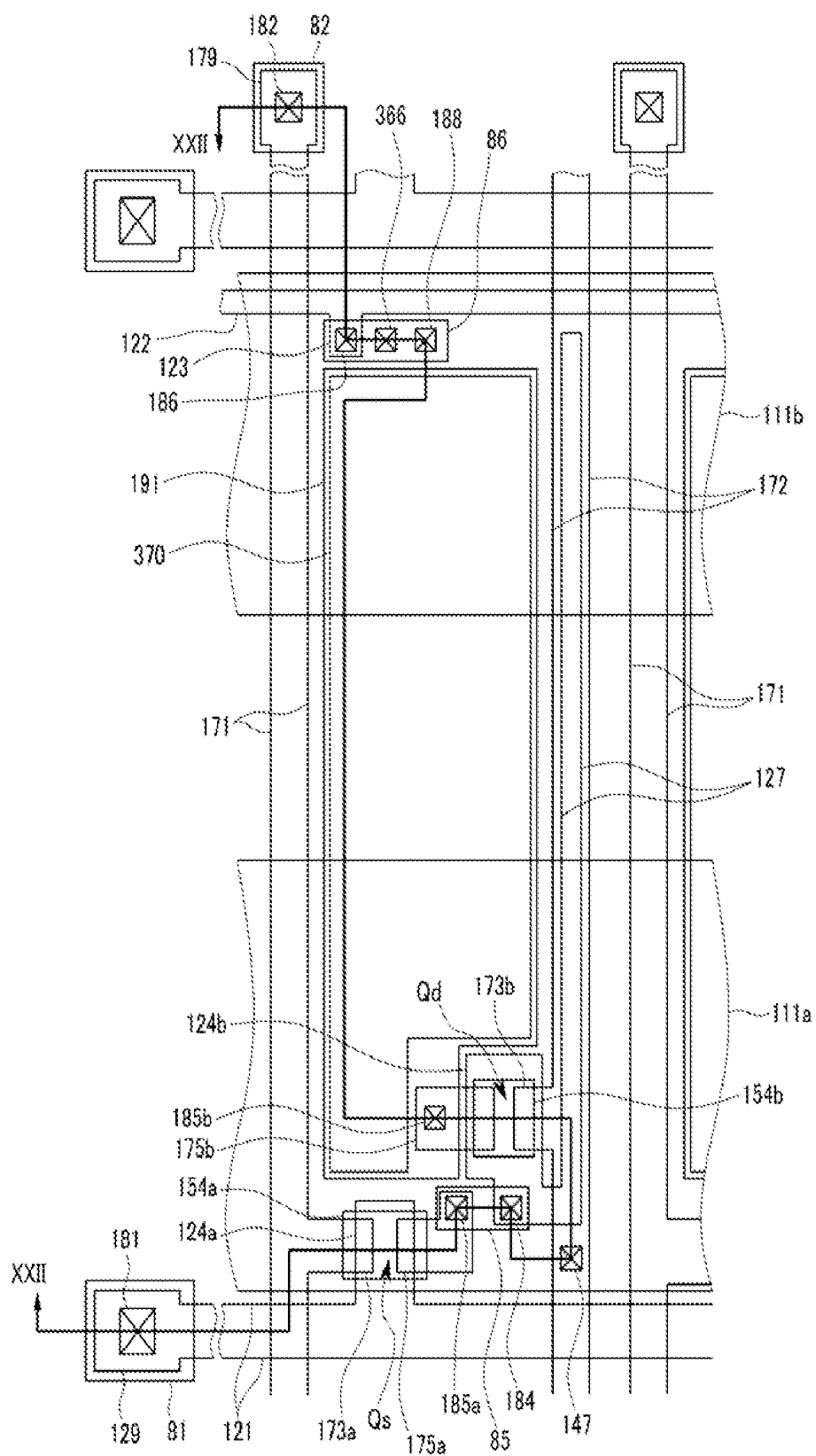
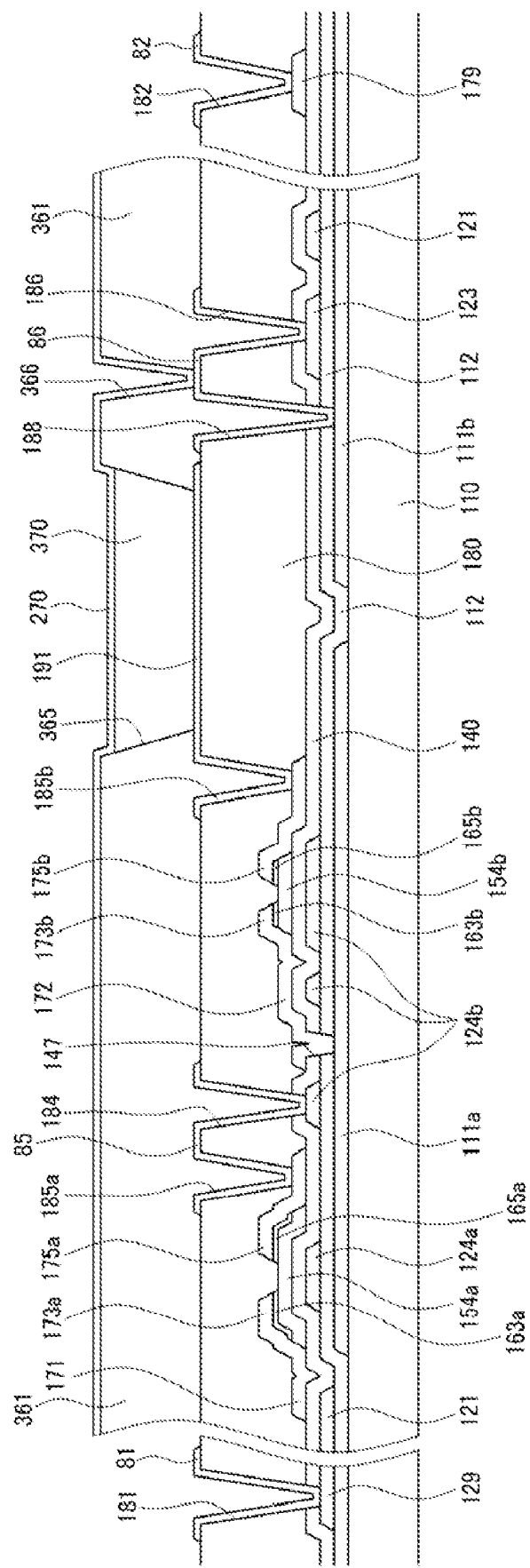


FIG.22



ORGANIC LIGHT-EMITTING DIODE DISPLAY**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims priority from and the benefit of Korean Patent Application No. 10-2005-0109063, filed on Nov. 15, 2005, and is a continuation-in-part of application Ser. No. 11/204,042, filed on Aug. 16, 2005, which is a continuation of application Ser. No. 10/732,280, filed on Dec. 11, 2003, now issued as U.S. Pat. No. 6,946,791, which claims priority from and the benefit of Korean Patent Application No. 10-2002-0078744, filed on Dec. 11, 2002, which are incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an organic light-emitting diode (OLED) display and a manufacturing method thereof.

[0004] 2. Discussion of the Background

[0005] The recent trend toward lightweight and thin personal computers and television sets requires lightweight and thin display devices. Hence, flat panel displays are replacing conventional cathode ray tubes (CRT). Flat panel displays include a liquid crystal display (LCD), a field emission display (FED), an organic light-emitting diode (OLED) display, and a plasma display panel (PDP). Among flat panel displays, the OLED display is the most promising because of its low power consumption, fast response time, wide viewing angle, and high contrast ratio. An OLED display is a self-emissive display device that includes an organic light-emitting layer interposed between two electrodes. One electrode injects holes and the other injects electrons into the light-emitting layer. The injected electrons and holes combine to form excitons, which emit light as they discharge energy. An OLED display may be a passive matrix display or an active matrix display according to its driving method. The passive matrix OLED display includes a plurality of anode lines, a plurality of cathode lines crossing the anode lines, and a plurality of pixels, each including a light emission layer. Selecting one anode line and one cathode line causes light emission of the pixel located at the intersection of the selected signal lines. The active matrix OLED display includes a plurality of pixels, and each pixel may include a switching transistor, a driving transistor, and a storage capacitor, as well as an anode, a cathode, and a light emission layer. The driving transistor receives a data voltage from the switching transistor and drives a current having a magnitude corresponding to the data voltage. The current from the driving transistor enters the light emission layer to cause light to emit at an intensity that depends on the current.

[0006] Here, input terminals of the driving transistors are commonly connected to driving voltage lines, which supply a driving voltage to the respective driving transistors. Hence, the magnitude of the current flowing through each driving transistor may be defined by the driving voltage as well as the data voltage. In other words, the magnitude of the current may be defined by a difference between the driving voltage and the data voltage.

[0007] However, with a larger OLED display, the driving voltages applied to the respective driving transistors may not

be uniform. Therefore, when data voltages of equal magnitude are applied to the driving transistors, the driving transistors may not output equal driving currents due to voltage drop, etc. Consequently, the same data voltage may result in different gray scales for displaying images.

[0008] Accordingly, a difference between driving voltages due to voltage drop may cause cross-talk, which deteriorates image quality.

SUMMARY OF THE INVENTION

[0009] The present invention provides a display device that may provide a substantially uniform driving voltage and/or common voltage.

[0010] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0011] The present invention discloses an organic light-emitting diode (OLED) display that includes a substrate, an auxiliary electrode disposed on the substrate, a first signal line disposed on the substrate, and a second signal line crossing the first signal line. A driving voltage line is disposed on the substrate, a first thin film transistor is connected to the first signal line and the second signal line, and a second thin film transistor is connected to the first thin film transistor and the driving voltage line. A first electrode is connected to the second thin film transistor, a second electrode faces the first electrode, and a light-emitting member is disposed between the first electrode and the second electrode. The auxiliary electrode is connected to at least one of the driving voltage line and the second electrode.

[0012] The present invention also discloses an OLED display that includes a substrate, a first auxiliary electrode disposed on the substrate, a first signal line disposed on the substrate, and a second signal line crossing the first signal line. A driving voltage line is connected to the first auxiliary electrode, a first thin film transistor is connected to the first signal line and the second signal line, and a second thin film transistor is connected to the first thin film transistor and the driving voltage line. A first electrode is connected to the second thin film transistor, a second electrode faces the first electrode, and a light-emitting member is disposed between the first electrode and the second electrode.

[0013] The present invention also discloses an OLED display, that includes a substrate, an auxiliary electrode disposed on the substrate, a first signal line disposed on the substrate, and a second signal line crossing the first signal line. A first thin film transistor is connected to the first signal line and the second signal line, and a second thin film transistor is connected to the first thin film transistor. A first electrode is connected to the second thin film transistor, a second electrode faces the first electrode and is connected to the auxiliary electrode, and a light-emitting member is disposed between the first electrode and the second electrode.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are included to provide a further understanding of the invention and are

incorporated in and constitute a part of this specification, illustrate embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0016] FIG. 1 is an equivalent circuit diagram of an OLED display according to exemplary embodiments of the present invention.

[0017] FIG. 2 is a layout view of an OLED display according to a first exemplary embodiment of the present invention.

[0018] FIG. 3 and FIG. 4 are sectional views of the OLED display of FIG. 2 taken along lines III-III and IV-IV, respectively.

[0019] FIG. 5, FIG. 8, FIG. 1, and FIG. 14 are layout views of the OLED display of FIG. 2, FIG. 3, and FIG. 4 showing intermediate steps of a manufacturing method thereof according to a first exemplary embodiment of the present invention.

[0020] FIG. 6 and FIG. 7 are sectional views of the OLED display of FIG. 5 taken along lines VI-VI and VII-VII, respectively.

[0021] FIG. 9 and FIG. 10 are sectional views of the OLED display of FIG. 8 taken along lines IX-IX and X-X, respectively.

[0022] FIG. 12 and FIG. 13 are sectional views of the OLED display of FIG. 1 taken along lines XII-XII and XIII-XIII, respectively.

[0023] FIG. 15 and FIG. 16 are sectional views of the OLED display of FIG. 14 taken along lines XV-XV and XVI-XVI, respectively.

[0024] FIG. 17 and FIG. 18 are layout views of an OLED display according to a second exemplary embodiment of the present invention.

[0025] FIG. 19 is a layout view of an OLED display according to a third exemplary embodiment of the present invention.

[0026] FIG. 20 is a sectional view of the OLED of FIG. 19 taken along line XX-XX.

[0027] FIG. 21 is a layout view of an OLED display according to a fourth exemplary embodiment of the present invention.

[0028] FIG. 22 is a sectional view of the OLED of FIG. 21 taken along line XXII-XXII.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0029] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various ways, all without departing from the spirit or scope of the invention. Therefore, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art.

[0030] In the drawings, the size and relative sizes of layers, films, panels, regions, etc., may be exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" or "connected to" another element, it can be directly on or directly connected to the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly connected to" another element, there are no intervening elements present.

[0031] FIG. 1 is an equivalent circuit diagram of an OLED display according to exemplary embodiments of the present invention.

[0032] Referring to FIG. 1, the OLED display includes a plurality of signal lines 121, 171, and 172. A plurality of pixels PX are connected to the signal lines 121, 171, and 172 and arranged substantially in a matrix.

[0033] The signal lines include a plurality of gate lines 121, which transmit gate signals (or scanning signals), a plurality of data lines 171, which transmit data signals, and a plurality of driving voltage lines 172, which transmit a driving voltage. The gate lines 121 extend substantially in a row direction and substantially parallel to each other, while the data lines 171 and the driving voltage lines 172 extend substantially in a column direction and substantially parallel to each other.

[0034] Each pixel PX includes a switching transistor Qs, a driving transistor Qd, a capacitor Cst, and an OLED LD.

[0035] The switching transistor Qs has a control terminal connected to a gate line 121, an input terminal connected to a data line 171, and an output terminal connected to the driving transistor Qd. The switching transistor Qs transmits the data signals applied to the data line 171 to the driving transistor Qd in response to the gate signal applied to the gate line 121.

[0036] The capacitor Cst is connected between the control terminal and the input terminal of the driving transistor Qd. The capacitor Cst stores the data signal applied to the control terminal of the driving transistor Qd and maintains the data signal after the switching transistor Qs turns off.

[0037] The OLED LD has an anode connected to the output terminal of the driving transistor Qd and a cathode connected to a common voltage Vss. The OLED LD emits light having an intensity depending on an output current ILD of the driving transistor Qd, thereby displaying images.

[0038] The switching transistor Qs and the driving transistor Qd are n-channel field effect transistors (FETs). However, at least one of the switching transistor Qs and the driving transistor Qd may be a p-channel FET. Additionally, the connections among the transistors Qs and Qd, the capacitor Cst, and the OLED LD may be modified.

[0039] A detailed structure of the OLED display of FIG. 1 according to an exemplary embodiment of the present invention will be described in detail below with reference to FIG. 2, FIG. 3, and FIG. 4.

[0040] FIG. 2 is a layout view of an OLED display according to a first embodiment of the present invention, and

FIG. 3 and FIG. 4 are sectional views of the OLED display of FIG. 2 taken along lines III-III and IV-IV, respectively.

[0041] An auxiliary electrode 111 is formed on an insulating substrate 110, which may be made of a material such as transparent glass or plastic. The auxiliary electrode 111 may have a substantially planar shape, and it may cover the entire a mother substrate (not shown). When the OLED display is a bottom emission type, the auxiliary electrode 111 may be made of a transparent or translucent conductor such as indium tin oxide (ITO) or indium zinc oxide (IZO), etc. Alternatively, when the OLED display is a top-emission type, the auxiliary electrode 111 may be made of a low resistivity conductor including Al, Ag, Cu, or alloys thereof.

[0042] A blocking layer 112, which may be made of silicon nitride (SiNx) or silicon oxide (SiOx), etc., is formed on the auxiliary electrode 111.

[0043] A plurality of gate conductors that include a plurality of gate lines 121 and a plurality of second control electrodes 124b are formed on the blocking layer 112. The gate lines 121 include first control electrodes 124a.

[0044] The gate lines 121 transmit gate signals and extend substantially in a transverse direction. Each gate line 121 further includes an end portion 129, which has a large area for connecting to another layer or an external driving circuit, and the first control electrodes 124a, which project upward from the gate line 121. The gate lines 121 may extend to be directly connected to a gate driving circuit (not shown) for generating the gate signals, which may be integrated on the substrate 110.

[0045] Each second control electrode 124b is spaced apart from the gate lines 121 and includes a storage electrode 127, which extends downward from the second control electrode 124b, turns to the right, and extends upward as shown in FIG. 2.

[0046] The gate conductors 121 and 124b may be made of Al, Ag, Cu, Mo or an alloy thereof, Cr, Ta, Ti, etc. The gate conductors 121 and 124b may have a multi-layered structure including two films having different physical characteristics from each other.

[0047] The lateral sides of the gate conductors 121 and 124b are inclined at an angle ranging from about 30 to 80 degrees relative to a surface of the substrate 110.

[0048] A gate insulating layer 140, which may be made of silicon nitride (SiNx) or silicon oxide (SiOx), is formed on the gate conductors 121 and 124b. The gate insulating layer 140 and the blocking layer 112 have a plurality of contact holes 147 exposing portions of the auxiliary electrode 111.

[0049] A plurality of first and second semiconductor islands 154a and 154b, which may be made of hydrogenated amorphous silicon ("a-Si") or polysilicon, are formed on the gate insulating layer 140. The first and second semiconductor islands 154a and 154b are disposed on the first and second control electrodes 124a and 124b, respectively.

[0050] A plurality of pairs of first ohmic contact islands 163a and 165a and a plurality of pairs of second ohmic contact islands 163b and 165b are formed on the first and second semiconductor islands 154a and 154b, respectively. The ohmic contacts 163a, 163b, 165a, and 165b may be

made of silicide or n+ hydrogenated a-Si heavily doped with an n-type impurity such as phosphorous.

[0051] A plurality of data conductors, which include a plurality of data lines 171, a plurality of driving voltage lines 172, and a plurality of first and second output electrodes 175a and 175b, are formed on the ohmic contacts 163a, 163b, 165a, and 165b and the gate insulating layer 140.

[0052] The data lines 171, which transmit data signals, extend substantially in the longitudinal direction and cross the gate lines 121. Each data line 171 includes a plurality of first input electrodes 173a extending toward the first control electrodes 124a and an end portion 179, which has a large area for connecting to another layer or an external driving circuit. The data lines 171 may extend to be directly connected to a data driving circuit (not shown) for generating the data signals, and the data driving circuit may be integrated on the substrate 110.

[0053] The driving voltage lines 172, which transmit driving voltages, extend substantially in the longitudinal direction and cross the gate lines 121. Each driving voltage line 172 includes a plurality of second input electrodes 173b extending toward the second control electrodes 124b. The driving voltage lines 172 overlap the storage electrodes 127.

[0054] The driving voltage lines 172 are connected to the auxiliary electrode 111 through the contact holes 147. The driving voltage lines 172 and the auxiliary electrode 111 are supplied with the same voltage. Consequently, driving voltages applied to the pixels may be substantially equal to each other. Moreover, although the auxiliary electrode 111 has sheet resistance, and a voltage applied to the auxiliary electrode 111 drops due to surface resistance, voltages applied to the respective pixels may be almost uniformly maintained. Therefore, substantially uniform voltages may be applied to the pixels such that image deterioration, such as a cross-talk due to a luminance difference of pixels, largely decreases.

[0055] The first and second output electrodes 175a and 175b are spaced apart from each other and from the data lines 171 and the driving voltage lines 172. Each pair of a first input electrode 173a and a first output electrode 175a are disposed opposing each other with respect to a first control electrode 124a, and each pair of a second input electrode 173b and a second output electrode 175b are disposed opposing each other with respect to a second control electrode 124b.

[0056] The data conductors 171, 172, 175a, and 175b may be made of a refractory metal including Mo, Cr, Ta, Ti, or alloys thereof. They may have a multi-layered structure including a refractory metal film and a low resistivity film.

[0057] Similar to the gate conductors 121 and 124b, lateral sides of the data conductors 171, 172, 175a, and 175b are inclined at an angle ranging from about 30 to 80 degrees relative to a surface of the substrate 110.

[0058] A passivation layer 180 is formed on the data conductors 171, 172, 175a, and 175b, the exposed portions of the semiconductor islands 154a and 154b, and the gate insulating layer 140.

[0059] The passivation layer 180 may be made of an inorganic or organic insulator, and it may have a substantially flat top-surface. Examples of the inorganic insulator

include silicon nitride and silicon oxide, and an example of the organic insulator includes a polyacryl. The passivation layer may include two or more layers. For example, the passivation layer **180** may have a double-layered structure including a lower film of an inorganic insulator and an upper film of an organic insulator.

[0060] The passivation layer **180** has a plurality of contact holes **182**, **185a**, and **185b** exposing the end portions **179** of the data lines **171**, the first output electrodes **175a**, and the second output electrodes **175b**, respectively, and the passivation layer **180** and the gate insulating layer **140** have a plurality of contact holes **181** and **184** exposing the end portions **129** of the gate lines **121** and the second control electrodes **124b**, respectively.

[0061] A plurality of pixel electrodes **191**, a plurality of connecting members **85**, and a plurality of contact assistants **81** and **82** are formed on the passivation layer **180**.

[0062] The pixel electrodes **191** are connected to the second output electrodes **175b** through the contact holes **185b**.

[0063] The connecting members **85** are connected to the second control electrodes **124b** and the first output electrodes **175a** through the contact holes **184** and **185a**, respectively.

[0064] The contact assistants **81** and **82** are connected to the end portions **129** of the gate lines **121** and the end portions **179** of the data lines **171** through the contact holes **181** and **182**, respectively. The contact assistants **81** and **82** protect the end portions **129** and **179** and enhance adhesion between the end portions **129** and **179** and external devices.

[0065] A partition **361** is formed on the passivation layer **180** to form a bank around the pixel electrodes **191**, thereby defining openings **365**. The partition **361** may be made of an organic material having thermal resistance and solvent resistance such as acrylic resin or polyimide resin, etc., or an inorganic insulating material such as SiO₂ or TiO₂, etc. The partition **361** may be made of a photosensitive material containing a black pigment so that the black partition **361** may serve as a light blocking member and it may be more easily formed.

[0066] A plurality of organic light-emitting members **370** are formed on the pixel electrodes **191**. The organic light-emitting members **370** may be confined in the openings **365** defined by the partition **361**.

[0067] Each organic light-emitting member **370** may have a multi-layered structure including a light emitting layer (not shown), which emits light, and one or more auxiliary layers (not shown), which improve the light-emitting layer's light emission efficiency.

[0068] The light-emitting layers may be made of an organic material or a mixture of an organic material and an inorganic material that emits light of one primary color such as red, green, or blue, or the light-emitting layers may include a compound doped with a polyfluorene derivative, a (poly)paraphenylenevinylene derivative, a polyphenylene derivative, a polyfluorene derivative, polyvinylcarbazole, a polythiophene derivative, or a compound made by adding a perylene-containing pigment, a cumarine-containing pigment, a rhodamine group pigment, rubrene, perylene, 9,10-diphenylanthracene, tetraphenylbutadiene, Nile red, cou-

marin, quinacridone, etc., to a high polymer of the derivatives. The OLED display displays images by spatially adding the monochromatic primary color lights emitted from the light-emitting layers.

[0069] The auxiliary layers (not shown) may include an electron transport layer (ETL) and a hole transport layer (HTL) to improve the balance of electrons and holes, and an electron injecting layer (EIL) and a hole injecting layer (HIL) to improve the injection of electrons and holes. The auxiliary layers may include one or more of such layers. The HTL and the HIL may be made of a material having a work function having a magnitude that is between that of the pixel electrode **191** and the light-emitting layer, and the ETL and the EIL may be made of a material having a work function that is between that of a common electrode **270** and the light-emitting layers. For instance, the HTL and the HIL may include poly-(3,4-ethylenedioxythiophene:polystyrenesulfonate (PEDOT:PSS), etc.

[0070] The common electrode **270** is formed on the organic light-emitting members **370** and the partition **361**. The common electrode **270** is formed on the entire surface of the organic light-emitting members **370**, and it applies a current to the organic light-emitting member **370** together with the pixel electrodes **191**.

[0071] In an OLED display such as described above, a first control electrode **124a** connected to a gate line **121**, a first input electrode **173a** connected to a data line **171**, and a first output electrode **175a**, along with a first semiconductor island **154a**, form a switching TFT Qs having a channel formed in the first semiconductor island **154a** disposed between the first input electrode **173a** and the first output electrode **175a**. Likewise, a second control electrode **124b** connected to a first output electrode **175a**, a second input electrode **173b** connected to a driving voltage line **172**, and a second output electrode **175b** connected to a pixel electrode **191**, along with a second semiconductor island **154b**, form a driving TFT Qd having a channel formed in the second semiconductor island **154b** disposed between the second input electrode **173b** and the second output electrode **175b**.

[0072] In the exemplary embodiment of FIG. 1 and FIG. 2, each pixel includes a switching TFT Qs and a driving TFT Qd, but the pixels may further include at least one transistor and a plurality of wires for driving the transistor such that deterioration of the organic light-emitting diode LD and the driving TFT Qd due to long-time driving is prevented or compensated, to prevent shortening the life of the OLED.

[0073] A pixel electrode **191**, an organic light-emitting member **370**, and the common electrode **270** form an OLED LD having the pixel electrode **191** as an anode and the common electrode **270** as a cathode, or vice versa. The overlapping portions of a storage electrode **127** and a driving voltage line **172** form a storage capacitor Cst.

[0074] Alternatively, the semiconductor islands **154a** and **154b** may be made of polysilicon. In this case, they may include intrinsic regions (not shown) disposed under the gate electrodes **124a** and **124b** and extrinsic regions (not shown) disposed opposing each other with respect to the intrinsic regions. The extrinsic regions are connected to the input electrodes **173a** and **173b** and the output electrodes **175a** and **175b**, and the ohmic contacts **163a**, **163b**, **165a**, and **165b** may be omitted.

[0075] Further, the gate electrodes **124a** and **124b** may be disposed over the semiconductor islands **154a** and **154b**, while the gate insulating layer **140** is still interposed between the semiconductor islands **154a** and **154b** and the gate electrodes **124a** and **124b**. Here, the data conductors **171**, **172**, **173b** and **175b** may be disposed on the gate insulating layer **140** and connected to the semiconductor islands **154a** and **154b** through contact holes (not shown) in the gate insulating layer **140**. Otherwise, the data conductors **171**, **172**, **173b**, and **175b** may be disposed under the semiconductor islands **154a** and **154b** and may contact the semiconductor islands **154a** and **154b**.

[0076] A method of manufacturing the OLED display shown in FIGS. 2-4 is described below with reference to FIGS. 5-16, as well as FIGS. 2-4, according to an exemplary embodiment of the present invention.

[0077] FIG. 5, FIG. 8, FIG. 11, and FIG. 14 are layout views of the OLED display of FIG. 2, FIG. 3, and FIG. 4 in intermediate steps of a manufacturing method thereof according to an exemplary embodiment of the present invention. FIG. 6 and FIG. 7 are sectional views taken along lines VI-VI and VII-VII of FIG. 5, respectively. FIG. 9 and FIG. 10 are sectional views taken along lines IX-IX and X-X of FIG. 8, respectively. FIG. 12 and FIG. 13 are sectional views taken along lines XII-XII and XIII-XIII of FIG. 11, respectively. FIG. 15 and FIG. 16 are sectional views taken along lines XV-XV and XVI-XVI of FIG. 14, respectively.

[0078] Referring to FIG. 5, FIG. 6, and FIG. 7, an auxiliary electrode **111**, which may be made of a conductor such as ITO, IZO, etc., is formed on a substrate **110**. For example, the auxiliary electrode **111** may be formed by disposing a shadow mask on the substrate **110** and depositing the conductor. Alternatively, the conductor may be deposited on the entire surface of the substrate **110** and portions of the conductor on ends of the substrate **110** may be removed.

[0079] Next, a blocking layer **112**, which may be made of silicon nitride, is formed on the auxiliary electrode **111**.

[0080] Gate conductors that include a plurality of gate lines **121** and a plurality of second control electrodes **124b** are formed on the blocking layer **112**. The gate lines **121** include first control electrodes **124a** and end portions **129**, and the second control electrodes **124b** include storage electrodes **127**. The gate conductors are preferably made of an Al alloy.

[0081] Referring to FIG. 8, FIG. 9, and FIG. 10, after sequentially depositing a gate insulating layer **140**, an intrinsic a-Si layer, and an extrinsic a-Si layer on the gate insulating layer **140**, the extrinsic a-Si layer and the intrinsic a-Si layer are patterned by photolithography and etched to form a plurality of extrinsic semiconductor islands (not shown) and a plurality of intrinsic semiconductor islands **154a** and **154b**.

[0082] The gate insulating layer **140** and the blocking layer **112** may be patterned by photolithography to form a plurality of contact holes **147**.

[0083] Data conductors that include a plurality of data lines **171**, a plurality of driving voltage lines **172**, and a plurality of first and second output electrodes **175a** and **175b** are preferably made of an Al alloy. The data lines **171** include first input electrodes **173a** and end portions **179**, and

the driving voltage lines **172** include second input electrodes **173b**. Here, the driving voltage lines **172** are connected to the auxiliary electrode **111** through the contact holes **147**.

[0084] Thereafter, portions of the extrinsic semiconductor islands, which are not covered with the data conductors **171**, **172**, **175a**, and **175b**, may be removed by etching to complete a plurality of ohmic contact islands **163a**, **163b**, **165a**, and **165b** and to expose portions of the intrinsic semiconductor islands **154a** and **154b**.

[0085] Referring to FIG. 11, FIG. 12, and FIG. 13, a passivation layer **180** is deposited and patterned by photolithography and etching using chemical vapor deposition or a printing process to form a plurality of contact holes **181**, **182**, **184**, **185a** and **185b**. The contact holes **181**, **182**, **184**, **185a**, and **185b** expose the end portions **129** of the gate lines **121**, the end portions **179** of the data lines **171**, the second control electrodes **124b**, the first output electrodes **175a**, and the second output electrodes **175b**, respectively.

[0086] Next, referring FIG. 11, FIG. 12, and FIG. 13, a plurality of pixel electrodes **191**, a plurality of connecting members **85**, and a plurality of contact assistants **81** and **82** are formed on the passivation layer **180**.

[0087] Referring to FIG. 14, FIG. 15, and FIG. 16, after depositing a photosensitive organic insulator using spin coating, the insulator is exposed and developed by photolithography to form a partition **361** having openings **365** on the pixel electrodes **191**.

[0088] Thereafter, a plurality of organic light-emitting members **370**, each of which includes an HTL (not shown) and a light-emitting layer (not shown), are formed on the pixel electrodes **191** and confined in the openings **365**.

[0089] The organic light-emitting members **370** may be formed by a solution process such as an inkjet printing or a deposition process. The organic light-emitting members **370** may be formed by inkjet printing, which deposits a solution into the openings **365** while moving an inkjet head (not shown). In this case, a drying step for removing solvent follows the deposition process.

[0090] Next, referring to FIG. 2, FIG. 3, and FIG. 4, a common electrode **270** is formed on the partitions **361** and the organic light-emitting members **370**.

[0091] A second exemplary embodiment of the present invention, of which portions are modified with respect to the above-described first exemplary embodiment, will be described below with reference to FIG. 17 and FIG. 18.

[0092] FIG. 17 and FIG. 18 are layout views showing an OLED display according to the second exemplary embodiment of the present invention.

[0093] Referring to FIG. 17, an auxiliary electrode **111** is formed so that it does not overlap the gate lines **121**, as opposed to the first exemplary embodiment in which the auxiliary electrode **111** is formed on the entire surface of the mother substrate. Not overlapping the auxiliary electrode **111** and the gate lines **121** may prevent a short-circuit between the auxiliary electrode **111** and the gate lines **121**.

[0094] Referring to FIG. 18, the auxiliary electrode **111** is formed between the gate lines **121** and the light-emitting regions, which correspond to the light-emitting layers of the organic light-emitting members **370**. When the above struc-

ture is applied, even though the OLED is a bottom emission type, the light-emitting regions are not covered by the auxiliary electrode 111. Hence, the auxiliary electrode 111 may be an opaque conductor. Therefore, when the OLED is the bottom emission type, the auxiliary electrode 111 may be formed of a low resistivity conductor such as Al, Ag, Cu, or an alloy thereof, to reduce resistance.

[0095] The other elements except for the auxiliary electrode 111 are the same as those of the first exemplary embodiment. Detailed descriptions of the elements are therefore omitted.

[0096] An OLED display of a top-emission type according to a third exemplary embodiment of the present invention will be described below with reference to FIG. 19 and FIG. 20, as well as FIG. 1. Descriptions of the same elements as those of the above-described embodiments are omitted.

[0097] FIG. 19 is a layout view of an OLED display according to a third exemplary embodiment of the present invention, and FIG. 20 is a sectional view taken along line XX-XX of FIG. 19.

[0098] An auxiliary electrode 111 is formed on an insulating substrate 110. The auxiliary electrode 111 may have a substantially planar shape, and it may cover the entire surface of a mother substrate (not shown). The auxiliary electrode 111 may be made of a low resistivity conductor including Al, Ag, Cu, or alloys thereof.

[0099] A blocking layer 112 is formed on the auxiliary electrode 111.

[0100] A plurality of gate conductors that include a plurality of gate lines 121, a plurality of second control electrodes 124b, and a plurality of voltage auxiliary lines 122 are formed on the blocking layer 112. The gate lines 121 include first control electrodes 124a, and the voltage auxiliary lines 122 include protrusions 123.

[0101] The voltage auxiliary lines 122 transmit a common voltage and extend substantially in parallel with the gate lines 121. The protrusions 123 extend downward from each auxiliary electrode line 122.

[0102] The gate insulating layer 140 is formed on the gate conductors 121, 124b, and 122.

[0103] A plurality of first and second semiconductor islands 154a and 154b are formed on the gate insulating layer 140. A plurality of pairs of first ohmic contact islands 163a and 165a and a plurality of pairs of second ohmic contact islands 163b and 165b are formed on the first and second semiconductor islands 154a and 154b, respectively.

[0104] A plurality of data conductors, which include a plurality of data lines 171, a plurality of driving voltage lines 172, and a plurality of first and second output electrodes 175a and 175b, are formed on the ohmic contacts 163a, 163b, 165a, and 165b and the gate insulating layer 140.

[0105] Unlike the above-described embodiments, the driving voltage lines 172 are not connected to the auxiliary electrode 111.

[0106] Alternatively, instead of forming the voltage auxiliary lines 122 on the same layer as the gate lines 121, the voltage auxiliary lines may be formed on the same layer as the data lines 171, the driving voltage lines 172, and the first

and second output electrode 175a and 175b. In this case, the voltage auxiliary lines may extend substantially in parallel with the data lines 171.

[0107] A passivation layer 180 is formed on the data conductors 171, 172, 175a, and 175b, the exposed portions of the semiconductor islands 154a and 154b, and the gate insulating layer 140.

[0108] The passivation layer 180 has a plurality of contact holes 182, 185a, and 185b exposing the end portions 179 of the data lines 171, the first output electrodes 175a, and the second output electrodes 175b, respectively, and the passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181, 184, and 186 exposing the end portions 129 of the gate lines 121, the second control electrodes 124b, and the protrusions 123 of the voltage auxiliary lines 122, respectively. Furthermore, the passivation layer 180, the gate insulating layer 140, and the blocking layer 112 have a plurality of contact holes 188 exposing the auxiliary electrode 111.

[0109] A plurality of pixel electrodes 191, a plurality of connecting members 85 and 86, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[0110] They may have a single-layered structure, which may be made of an opaque conductor, or a double-layered structure of ITO and an opaque conductor. The opaque conductor may be made of Al, Au, Pt, Ni, Cu, W, or alloys thereof having a high work function.

[0111] The connecting members 85 are connected to the second control electrodes 124b and the first output electrodes 175a through the contact holes 184 and 185a, respectively.

[0112] The connecting members 86 are connected to the protrusions 123 of the voltage auxiliary lines 122 and the auxiliary electrodes 111 through the contact holes 186 and 188, respectively.

[0113] A partition 361, which has openings 365 and contact holes 366, is formed on the passivation layer 180, and a plurality of organic light-emitting members 370 are formed within the openings 365.

[0114] A common electrode 270 is formed on the entire surface of the substrate including the partition 361 and the organic light-emitting members 370. The common electrode 270 may be made of a transparent or translucent conductive material having a good electron injection characteristic and that does not negatively affect an organic material. Examples of the conductive materials include a 50 to 100 Å thick, single-layered structure of ITO, IZO, Al, and Ag, or a multi-layered structure of Ca—Ag, LiF—Al, Ca—Ba, and Ca—Ag-ITO. Because the common electrode 270 is made of transparent or translucent conductive material, light may be emitted toward the top of the substrate 110 on which thin film transistors are formed.

[0115] The common electrode 270 is connected to the protrusions 123 of the voltage auxiliary lines 122 through the contact holes 366 and the connecting members 86. Hence, the common electrode 270, the protrusions 123 of the voltage auxiliary lines 122, and the auxiliary electrode 111 are connected to each other.

[0116] Such connections may permit the common electrode 270 to stably supply a common voltage when the

common electrode 270 is made of a high resistivity transparent or translucent conductive material. Consequently, the common voltage applied to the entire area of the common electrode 270 may be substantially uniform (i.e. without a voltage drop), to reduce cross-talk due to a luminance difference between pixels.

[0117] A fourth exemplary embodiment of the present invention, of which portions are modified with respect to the above described first embodiment of FIGS. 1 to 4, will be described below with reference to FIG. 21 and FIG. 22. The descriptions of the same elements as those of the above-described embodiments are omitted.

[0118] FIG. 21 is a layout view of an OLED display according to a fourth exemplary embodiment of the present invention, and FIG. 22 is a sectional view taken along line XXII-XXII of FIG. 21.

[0119] Referring to FIG. 21 and FIG. 22, a first auxiliary electrode 111a and a second auxiliary electrode 111b are formed on an insulating substrate 110. The first and second auxiliary electrodes 111a and 111b are spaced apart from each other by a predetermined interval and have a substantially planar shape. The first and second auxiliary electrodes 111a and 111b may be made of a low resistivity conductor including Al, Ag, Cu, or alloys thereof.

[0120] A blocking layer 112 is formed on the first and second auxiliary electrodes 111a and 111b.

[0121] A plurality of gate conductors that include a plurality of gate lines 121, a plurality of second control electrodes 124b, and a plurality of voltage auxiliary lines 122 are formed on the blocking layer 112. The gate lines 121 include first control electrodes 124a, and the voltage auxiliary lines 122 include protrusions 123.

[0122] The gate insulating layer 140 is formed on the gate conductors 121, 124b, and 122.

[0123] The gate insulating layer 140 and the blocking layer 112 have a plurality of contact holes 147 exposing the first auxiliary electrode 111a.

[0124] A plurality of first and second semiconductor islands 154a and 154b are formed on the gate insulating layer 140. A plurality of pairs of first ohmic contact islands 163a and 165a and a plurality of pairs of second ohmic contact islands 163b and 165b are formed on the first and second semiconductor islands 154a and 154b, respectively.

[0125] A plurality of data conductors, which include a plurality of data lines 171, a plurality of driving voltage lines 172, and a plurality of first and second output electrodes 175a and 175b, are formed on the ohmic contacts 163a, 163b, 165a, and 165b and the gate insulating layer 140. The driving voltage lines 172 are connected to the first auxiliary electrode 111a through the contact holes 147.

[0126] A passivation layer 180 is formed on the data conductors 171, 172, 175a, and 175b, the exposed portions of the semiconductor islands 154a and 154b, and the gate insulating layer 140.

[0127] The passivation layer 180 has a plurality of contact holes 182, 185a, and 185b exposing the end portions 179 of the data lines 171, the first output electrodes 175a, and the second output electrodes 175b, respectively, and the passivation layer 180 and the gate insulating layer 140 have a

plurality of contact holes 181, 184, and 186 exposing the end portions 129 of the gate lines 121, the second control electrodes 124b, and the protrusions 123 of the voltage auxiliary lines 122, respectively. Furthermore, the passivation layer 180, the gate insulating layer 140, and the blocking layer 112 have a plurality of contact holes 188 exposing the second auxiliary electrode 111b.

[0128] A plurality of pixel electrodes 191, a plurality of connecting members 85 and 86, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[0129] The connecting members 85 are connected to the second control electrodes 124b and the first output electrodes 175a through the contact holes 184 and 185a, respectively.

[0130] The connecting members 86 are connected to the protrusions 123 of the voltage auxiliary lines 122 and the second auxiliary electrodes 111b through the contact holes 186 and 188, respectively.

[0131] A partition 361, which has openings 365 and contact holes 366, is formed on the passivation layer 180, and a plurality of organic light-emitting members 370 are formed within the openings 365.

[0132] A common electrode 270 is formed on the entire surface of the substrate including the partition 361 and the organic light-emitting members 370.

[0133] The common electrode 270 is connected to the protrusions 123 of the voltage auxiliary lines 122 through the contact holes 366 and the connecting members 86. Hence, the common electrode 270, the protrusions 123 of the voltage auxiliary lines 122, and the second auxiliary electrode 111b are connected to each other.

[0134] As described above, the first and second auxiliary electrodes 111a and 111b are formed on the substrate 110, the first auxiliary electrode 111a is connected to the driving voltage lines 172, and the second auxiliary electrodes 111b are connected to the common electrode 270. Accordingly, a driving voltage may be applied to the driving voltage lines 172 and the first auxiliary electrode 111a, and a common voltage may be applied to the common electrode 270 and the second auxiliary electrode 111b, so that the driving voltage and the common voltage may be uniformly applied to all pixels. Moreover, the first and second auxiliary electrodes 111a and 111b have sheet resistance. Hence, even though a voltage drop of the voltages applied to each of the pixels may occur, the voltages may not significantly vary because of compensation of the voltage drop by the sheet resistance. Accordingly, the driving voltage and the common voltage may be substantially uniformly applied to the pixels, and cross-talk due to luminance difference between pixels may decrease.

[0135] While the first and second auxiliary electrodes and the driving voltage lines or the common electrode are shown as being connected in a display area, they may alternatively be connected in other areas.

[0136] According to exemplary embodiments of the present invention, by forming at least one auxiliary electrode, a driving voltage and a common voltage may be substantially uniformly applied to the pixels, thereby decreasing cross-talk due to a luminance difference between pixels.

[0137] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light-emitting diode (OLED) display, comprising:

- a substrate;
- an auxiliary electrode disposed on the substrate;
- a first signal line disposed on the substrate;
- a second signal line crossing the first signal line;
- a driving voltage line disposed on the substrate;
- a first thin film transistor connected to the first signal line and the second signal line;
- a second thin film transistor connected to the first thin film transistor and the driving voltage line;
- a first electrode connected to the second thin film transistor;
- a second electrode facing the first electrode; and
- a light-emitting member disposed between the first electrode and the second electrode,

wherein the auxiliary electrode is connected to at least one of the driving voltage line and the second electrode.

2. The OLED display of claim 1, wherein the auxiliary electrode is disposed on a layer different from one of the driving voltage line and the second electrode.

3. An organic light-emitting diode (OLED) display, comprising:

- a substrate;
- a first auxiliary electrode disposed on the substrate;
- a first signal line disposed on the substrate;
- a second signal line crossing the first signal line;
- a driving voltage line connected to the first auxiliary electrode;
- a first thin film transistor connected to the first signal line and the second signal line;
- a second thin film transistor connected to the first thin film transistor and the driving voltage line;
- a first electrode connected to the second thin film transistor;
- a second electrode facing the first electrode; and
- a light-emitting member disposed between the first electrode and the second electrode.

4. The OLED display of claim 3, wherein the first auxiliary electrode is disposed on a layer different from the driving voltage line.

5. The OLED display of claim 3, further comprising a blocking layer disposed on the first auxiliary electrode.

6. The OLED display of claim 3, wherein the first auxiliary electrode covers the entire surface of the substrate.

7. The OLED display of claim 3, wherein the first auxiliary electrode comprises a transparent or translucent conductor.

8. The OLED display of claim 3, wherein the first auxiliary electrode is spaced apart from the first signal line.

9. The OLED display of claim 3, wherein the first auxiliary electrode is disposed corresponding to the light-emitting member.

10. The OLED display of claim 9, wherein the first auxiliary electrode comprises at least one of Al, an Al alloy, Cu, a Cu alloy, Ag, and an Ag alloy.

11. The OLED display of claim 3, further comprising a second auxiliary electrode spaced apart from the first auxiliary electrode, the second auxiliary electrode being connected to the second electrode.

12. The OLED display of claim 11, wherein the first auxiliary electrode and the second auxiliary electrode are disposed on the same layer.

13. The OLED display of claim 11, wherein the second auxiliary electrode receives a voltage having the same magnitude as what the second electrode receives.

14. The OLED display of claim 11, further comprising a voltage auxiliary line disposed on the same layer as the first signal line or the second signal line, the voltage auxiliary line being connected to the second electrode and the second auxiliary electrode.

15. The OLED display of claim 11, wherein the second electrode comprises a transparent or translucent conductor.

16. The OLED display of claim 15, wherein the second electrode comprises indium tin oxide or indium zinc oxide.

17. The OLED display of claim 3, further comprising a partition, the light-emitting member being disposed in an opening of the partition.

18. An organic light-emitting diode (OLED) display, comprising:

- a substrate;
- an auxiliary electrode disposed on the substrate;
- a first signal line disposed on the substrate;
- a second signal line crossing the first signal line;
- a first thin film transistor connected to the first signal line and the second signal line;
- a second thin film transistor connected to the first thin film transistor;
- a first electrode connected to the second thin film transistor;
- a second electrode facing the first electrode, the second electrode being connected to the auxiliary electrode; and
- a light-emitting member disposed between the first electrode and the second electrode.

19. The OLED display of claim 18, further comprising a voltage auxiliary line disposed on the same layer as the first signal line or the second signal line, the voltage auxiliary line being connected to the second electrode.

20. The OLED display of claim 18, wherein the second electrode comprises a transparent or translucent conductor.

21. The OLED display of claim 20, wherein the second electrode comprises indium tin oxide or indium zinc oxide.

专利名称(译)	有机发光二极管显示器		
公开(公告)号	US20070063936A1	公开(公告)日	2007-03-22
申请号	US11/557244	申请日	2006-11-07
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
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IPC分类号	G09G3/30		
CPC分类号	G09G3/3225 G09G2300/0426 H01L27/3276 G09G2320/0209 G09G2320/0223 G09G2300/043		
优先权	1020020078744 2002-12-11 KR 1020050109063 2005-11-15 KR		
其他公开文献	US7710019		
外部链接	Espacenet USPTO		

摘要(译)

一种有机发光二极管显示器，包括基板，设置在基板上的辅助电极，设置在基板上的第一信号线，与第一信号线交叉的第二信号线，设置在基板上的驱动电压线，连接第一信号线和第二信号线的第一薄膜晶体管，连接第一薄膜晶体管和驱动电压线的第二薄膜晶体管，连接第二薄膜晶体管的第一电极，第二电极面对第一电极和设置在第一电极和第二电极之间的发光构件。辅助电极连接到驱动电压线和第二电极中的一个。

